Remarks

The various parts of the Office Action (and other matters, if any) are discussed below under appropriate headings.

Entry of this reply is considered proper. It is believed that the reply raises no new issues, does not require an additional search and/or places the application in a better condition for allowance and/or appeal.

Claim Rejections - 35 USC § 103

Independent claims 1 and 16 have each been amended to recite, *inter alia*, the elements found in previously dependent claims 11 and 12. As is discussed more fully below, the cited references, taken alone or in combination, fail to disclose or fairly suggest the recited methods of forming a charge-trapping dielectric semiconductor device.

Claim 1, as amended, recites a method of forming a semiconductor device that includes, *inter alia*, forming a charge-trapping dielectric layer over a substrate, where the charge-trapping dielectric layer includes a tunneling layer, a charge-trapping layer, and an insulating layer. The recited method further includes using a photosensitive layer to pattern only a mask layer, and forming a conductive layer over the patterned mask layer and filling at least one mask space in the patterned mask layer.

Sitaram fails to disclose or fairly suggest forming a charge-trapping dielectric layer over a substrate, where the charge-trapping dielectric layer includes a tunneling layer, a charge-trapping layer, and an insulating layer. Rather, Sitaram discloses forming a floating gate device in which a polysilicon layer (12) is disposed between a gate dielectric layer (11) on one side and a silicide layer (16) and covering oxide or nitride layer (17) on the other side.

In addition, Sitaram fails to disclose or fairly suggest forming a conductive layer over a patterned mask layer and filling at least one mask space in the patterned mask layer. Rather, Sitaram discloses forming a thin titanium or cobalt layer (15) covering the side wall and base on an opening (14). After, the thin titanium or cobalt layer (15) is formed, a nonconductive layer 17 is formed to fill the remainder of opening (14). None of the cited references, including Boyd et al. and Huang, cure the deficiencies of Sitaram.

For at least these reasons, it is respectfully submitted that claim 1 and claims 2-5, 10, and 13-15 dependent therefrom distinguish patentably over the references of record. Accordingly, the rejections should be withdrawn.

Boyd et al. fails to disclose or fairly suggest forming a charge-trapping dielectric layer over a substrate, where the charge-trapping dielectric layer includes a tunneling layer, a charge-trapping layer, and an insulating layer. Rather, Boyd et al. discloses forming a MOSFET device having a gate conductor (141) disposed over a single gate oxide layer (149).

In addition, Boyd et al. fails to disclose or fairly suggest using a photosensitive layer to pattern only the mask layer. Rather, Boyd et al. discloses using a resist layer (148) to pattern a mask layer (138) and (131) and a pad oxide layer (135). None of the cited references, including Sitaram and Huang, cure the deficiencies of Sitaram.

For at least these reasons, it is respectfully submitted that claim 1 and claims 2-5, 10, and 13-15 dependent therefrom distinguish patentably over the references of record. Accordingly, the rejections should be withdrawn.

Claim 16, as amended, recites a method of forming a semiconductor device that includes, *inter alia*, forming a charge-trapping dielectric layer over a substrate, where the charge-trapping dielectric layer includes a tunneling layer, a charge-trapping layer, and an insulating layer.

Neither Boyd et al. nor Sitaram, taken alone or in combination with any of the other cited references, discloses or fairly suggests forming a charge-trapping dielectric layer over a substrate, where the charge-trapping dielectric layer includes a tunneling layer, a charge-trapping layer, and an insulating layer. Rather, as discussed above, Sitaram discloses forming a floating gate device, and Boyd et al. discloses forming a MOSFET device having a gate conductor disposed over a single gate oxide layer.

For at least these reasons, it is respectfully submitted that claim 16 distinguishes patentably over the references of record. Accordingly, the rejections should be withdrawn.

Conclusion

In view of the foregoing, request is made for timely issuance of a notice of allowance.

Respectfully submitted,

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